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February 18, 2004

Commissioner for Patents P.O.Box 1450 Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572 28 Davis Avenue Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/723,236 11/26/03

Chun Hsien Lin et al.

AN ADVANCED PROCESS CONTROL APPROACH FOR Cu INTERCONNECT WIRING SHEET RESISTANCE CONTROL

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on February 23, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date ____

- U.S. Patent 6,555,477 to Lu et al., "Method for Preventing Cu CMP Corrosion," discloses a method for preventing or reducing corrosion of copper containing semiconductor features during chemical mechanical polishing (CMP).
- U.S. Patent 6,372,632 to Yu et al., "Method to Eliminate Dishing of Copper Interconnects by the Use of a Sacrificial Oxide Layer," describes a copper polishing step followed by an oxide buffing step.
- J. Zhang et al., "Automated Process Control of Within-Wafer and Wafer-to-Wafer Uniformity in Oxide CMP," [online]
 March 2002, CMP MIC [retrieved on January 27, 2003] retrieved from URL: http://www.appliedmaterials.com/search97cgi/s97_sgi, describes a within wafer closed loop control with feed-forward and feed-backward of data to provide run-to-run control.
- U.S. Patent 6,405,144 to Toprac et al., "Method and Apparatus for Programmed Latency for Improving Wafer-to-Wafer Uniformity," discusses a method and an apparatus for implementing programmed latency for improved wafer-to-wafer uniformity.
- U.S. Patent 6,148,239 to Funk et al., "Process Control System Using Feed Forward Control Threads Based on Material Groups," discusses feed forward process control system used in semiconductor fabrication based on material groupings.

- U.S. Patent 6,335,286 to Lansford, "Feedback Control of Polish Buff Time as a Function of Scratch Count," discusses a CMP buffing process controlled by monitoring the scratch count on a process surface and feeding the data back to a process controller.
- U.S. Patent 5,719,495 to Moslehi, "Apparatus for Semi-conductor Device Fabrication Diagnosis and Prognosis," discloses an in-situ non-invasive method of determining physical properties such as sheet resistance and film thickness.
- U.S. Patent 6,528,818 to Satya et al., "Test Structures and Methods for Inspection of Semiconductor Integrated Circuits," describes process control achieved through test structures in a system for detecting defects.
- U.S. Patent 6,514,858 to Hause et al., "Test Structure for Providing Depth of Polish Feedback," discusses a test structure to minitor CMP polish depth.

Sincerely,

Stephen B. Ackerman,

Req. No. 37761

Form PTO-1449 Doctor Humber (Coaches) TSMC-02-992 10 INFORMATION DISCLOSURE CITATION IN AN APPLICATION Filhe Door (Uso soveral shoots if necessary) U. S. PATENT DOCUMENTS REMINAR DOCUMENT NUMBER DATE HULE ያኒኒሀሚዐክሚሊ <mark>ት</mark> CLUE MECLIE 438 692 438 634 70 a 8-4 700 438 324 58. 257 48 438 640 FOREIGN PATENT DOCUMENTS Translation OCCUMENT NUMBER CUTE COUNTRY CLUSS SUBCLASS YES OTHER DOCUMENTS (Including Author, Title, Date, Perlinent Pages, Etc.) EXAMER DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant